REMARKS

In response to the above-identified Final Office Action, the Applicant submits the below remarks and respectfully requests reconsideration of the application, as amended, in light of these remarks. The amendments place the application in condition for allowance or in better form for appeal and, thus, shall be entered under 37 C.F.R. 1.116.

The Examiner rejected claims 1-3 under 35 U.S.C. 102 (e) as being anticipated by U.S. Patent 6,303,448 (hereinafter Chang). The Examiner rejected claims 4-6 under 35 U.S.C. 103 (a) as being unpatentable over Chang in view of U.S. Patent 5,567,966 (hereinafter Hwang). In addition, the Examiner rejected claims 7-9 under 35 U.S.C 103 (a) as being unpatentable by U.S. Patent 5,712,503 (hereinafter Kim) in view of Chang. The Applicant respectfully traverses these rejections for the reasons set out below.

The Applicant contends that none of the cited references, alone or in combination, teaches or suggests all limitations of claim 1, or the other independent claims of the present application. The Applicant's argument shall be presented with respect to claim 1. However, these comments are applicable to the other independent claims of the present application, and the Examiner is respectfully requested to consider these comments and remarks when reviewing the other independent claims for allowability.

With respect to claim 1, Chang does not teach an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess. As illustrated in Figure 6, an extensions 66 is subjacent the dielectric layer 62. More specifically, the innermost side of extensions 66 is not adjacent to an outside surface of the recess, an innermost side of the extension is adjacent to an outside surface of the recess. The innermost side of the extension is subjacent the dielectric layer 62.

With respect to claim 4, Hwang does not disclose shortcomings of Chang and does not disclose an extension which extends to a more shallow depth within the

substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an innermost side of the extension is adjacent to an outside surface of the recess.

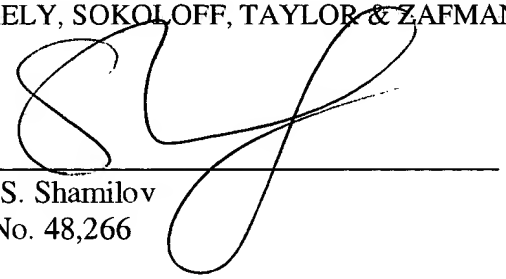
With respect to claim 7, Kim does not disclose a gate electrode completely overlying the gate dielectric layer and the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the curvilinear sides of the recess. As illustrated in figure 7, a dielectric layer 62 and 52 represent the same layer. The gate electrode 63 does not completely overlay the gate dielectric layer 62/52. In addition, Kim does not disclose the source/drain terminals comprising an extension. Kim discloses low concentration source/drain regions 60 and high concentration source/drain regions. Low concentration regions 63 do not constitute extensions in the source/drain terminals.

The Applicant submits that the rejections under 35 U.S.C. § 102 (e) and 103 (a) have been addressed, and withdrawal of these rejections is respectfully requested. The Applicant furthermore submits that all pending claims are in condition for allowance, which is earnestly solicited.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicants hereby request such an extension.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP



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MARKED UP VERSION OF THE CLAIMS

Please amend the following claims.

1. (Four Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having a bottom portion and substantially vertical sidewalls;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the substantially vertical sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls, said gate electrode extending to a less shallow depth within said substrate than a depth at which the source/drain terminals are disposed; wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate, along the sidewalls of the recess, an innermost side of the extension is adjacent to an outside surface of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension.

4. (Four Times Amended) A field effect transistor, comprising:

a substrate having a recess in a surface thereof, the recess having bottom portion and tapered sidewalls, the tapered sidewall surfaces forming an obtuse angle with respect to the bottom portions of the recess;

a gate dielectric layer disposed superjacent the bottom portion of the recess and adjacent the tapered sidewalls;

a gate electrode completely overlying the gate dielectric layer; and source/drain terminals disposed in the substrate in alignment with a pair of laterally opposed gate electrode sidewalls;

wherein the source/drain terminals comprise an extension which extends to a more shallow depth within the substrate than the source/drain terminals to which it corresponds and extends downwardly, from approximately the surface of the substrate,

along the sidewalls of the recess, an innermost side of the extension is adjacent to an outside surface of the recess, a portion of the gate dielectric layer overlaying an innermost portion of the extension.